Voltage Clamp: Design, Fabrication and Testing of a New and Improved Voltage Clamp Instrument[1]

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OBJECTIVE

To design a voltage clamp with improved performance and design in order to get accurate and precise I-V measurements of *Neurospora crassa* hyphae.

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ABSTRACT

Voltage clamping is used extensively to measure the current-voltage relations of cells by holding the voltage at a predefined level while observing the behavior of the clamping current. The accuracy and precision of the recordings are dependent on the voltage clamping circuit. The theory of such a design as well as the effect of feedback resistor values, were analyzed. Within error bounds there was no statistical difference from using feedback resistor values ranging from 1.23 MΩ - 1GΩ. There was a noticeable improvement between this design and the one constructed previously, there was better clamping fidelity at maximal clamping voltages.

INTRODUCTION

Operational amplifiers (Op Amps) are versatile devices for a wide number of applications since they are able to amplify the voltage or current by hundreds or thousands of times. Op Amp configurations can be implemented to get a variety of desired outputs. The following discussion focuses on the comparison between two voltage clamp designs and how the characteristics differ with regard to the electrical components used. These are an original voltage clamp circuit built a number of years ago, and the one that I designed and fabricated.

A general purpose LM741 Op Amp was used in a differential configuration to hold the voltage of the cell membrane at a predefined level while the clamping current was recorded. Any difference between the 'holding potential' and the membrane potential will cause a differential signal to be generated; it is amplified to inject current into the membrane to maintain the holding potential at the desired value.

$$A_v = gain = \frac{V_{sat}}{(V_+ - V_-)} \qquad (6)$$

$$(V_+ - V_-) = (15V / 10^5) = 150\mu V \qquad (7)$$

Where V_{out} is the output voltage, $V_{command}$ is the holding voltage predefined by the user and $V_{membrane}$ is the membrane potential of the cell. Since the gain of the Op Amp is relatively high due to the resistor values chosen, the output voltage will quickly peak to $\pm V_{saturated}$, where the saturation voltages are the maximum and minimum voltage at which the Op Amp circuit operates. The maximum and minimum voltages are provided by a power supply. Figure 1 shows the power supply circuit, where Vcc is set at ± 15 V; a typical range for Op Amp design. Note that the output is a voltage, but a voltage clamp requires that a current be injected into the cell to maintain the proper membrane potential. The current injection circuit was done by an electrometer (Warner Instruments model IE-

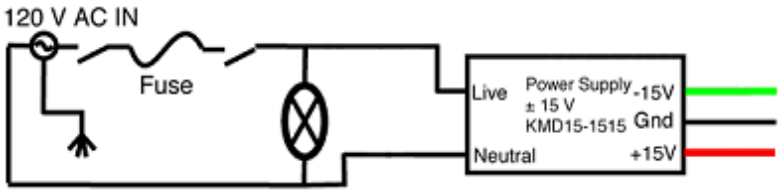


Figure 1: A KMD15-1515 power supply was used to convert the 120VAC to ±15VDC voltage.

251). It should be evident that an Op Amp works by amplifying the difference between the non-inverting and inverting inputs and in doing so produces a voltage output that equals ± Vcc. The two equations below define the output voltage with respect to the command (non-inverting) and monitor (inverting) inputs:

$$V_{command} = V^{+} > V_{monitor} = V^{-} \qquad V_{out} = +V_{cc} = +15V \qquad (2)$$

$$V_{command} = V^{+} < V_{monitor} = V^{-} \qquad V_{out} = -V_{cc} = -15V \qquad (3)$$

A 1 kΩ resistor connected between the command potential at the non-inverting input only serves to allow current protection in the case when the input voltage exceeds the supply voltage. Since the output impedance of the electrometer feeding into the command potential is only 100Ω, this addition is an important safety consideration. Although this is the case, theoretically the circuit will function without the 1kΩ resistor due to the very high input impedance ($10^{12}\Omega$) of the Op Amp. The output of the Op Amp is connected to the electrometer by either a TTL switch or a manual SPST (Single-Pole-Single-Throw) switch. The TTL switch is controlled via digital I/O provided by a Scientific Solutions Lab Master DMA that provides an interface with analog/digital (A/D), digital/analog (D/A), digital I/O and timer capabilities. The digital I/O from the computer controls whether the current will be injected into the cell. An ADG411 switch was used to connect the analog output of the voltage clamp circuit under digital I/O control. It has a fast switching time, low ON resistance and a signal range that extends to the ±15 V supply voltage (it has a built-in Op Amp with a Gain of 1 for this purpose). In the original voltage clamp circuit, a mechanical 5V relay was used, but due to the large moving relay head, the switching time is slower and less than suitable for our application. Furthermore, the ±15 V supply was upgraded to a medical grade KMD15-1515 power supply. It offered low peak-peak noise of 50 mV with a temperature coefficient of ±0.01%/°C. This ensured that the system was less affected by the inherent AC voltage noise although some could be detected and will be discussed further in the discussion. The output of this power supply was able to provide a maximum of 500 mA of current at ±15 V, which was more than sufficient for our needs. An NTE956 variable voltage regulator was used to provide an output voltage of +5V to drive the TTL logic of the ADG411 IC TTL switch (Figure 2 & 3). Equation 4 was used to choose the correct resistor values to obtain a +5V voltage, and (5) shows the corresponding output voltage that was as close to the +5V desired output as possible given the practical resistors that could be used. The 4.72 V output did not affect the performance or functionality of the system in any way.

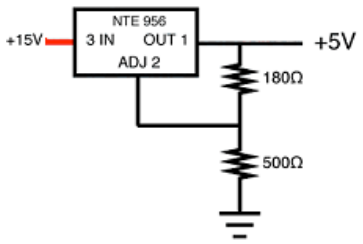


Figure 2: 5V Output Power Supply using a variable voltage regulator. Used for the integrated ADG411 switch.

$$V_{out} = 1.25V(1+\frac{R_2}{R_1}) \quad (4)$$

$$V_{out} = (4.72 \pm 0.01)V \quad (5)$$

The complete circuit is shown in Figure 3.

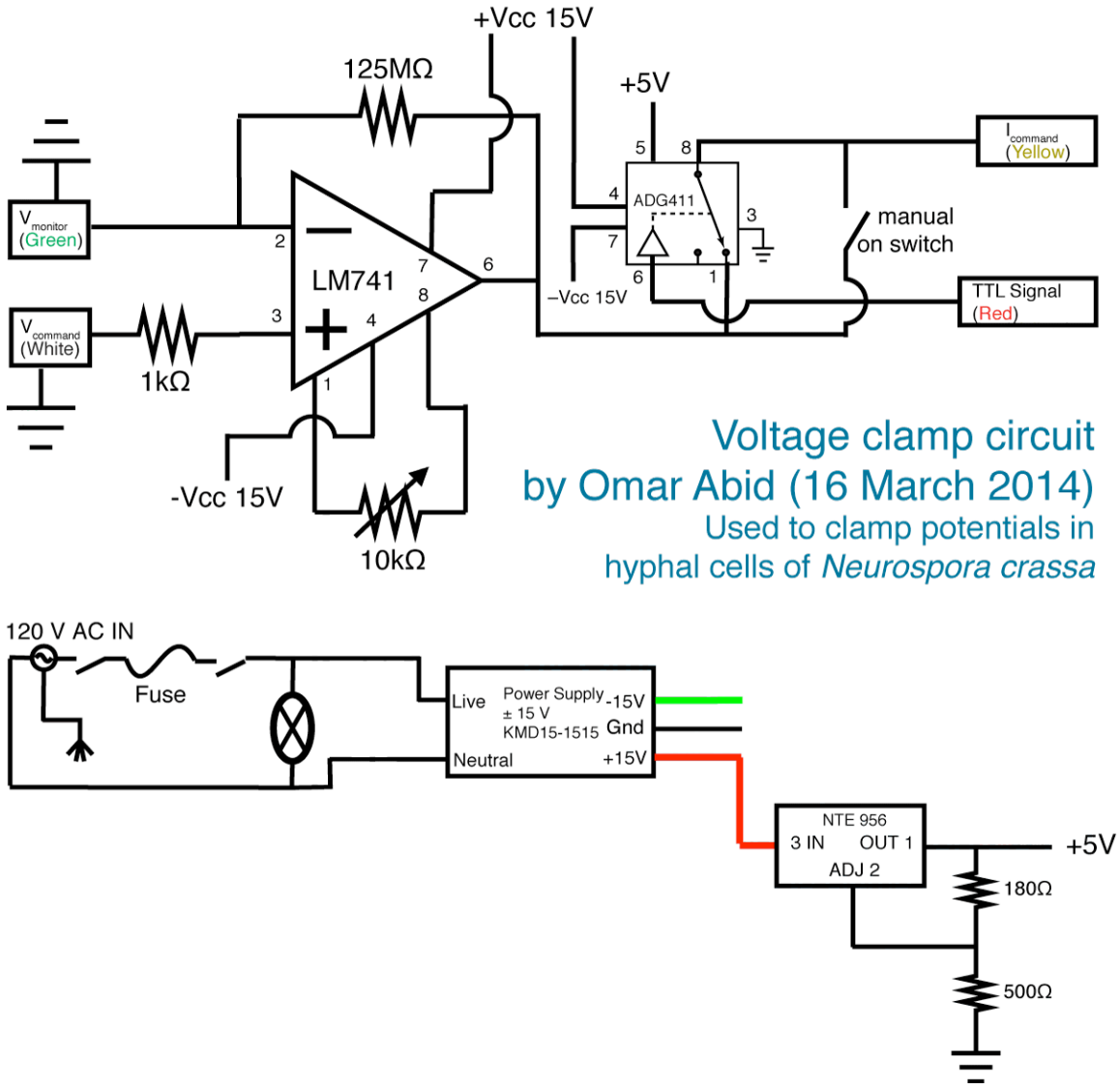


Figure 3: The voltage clamp circuit in a differential Op Amp configuration driven by ±15 V. The ADG411 can swing its output from $\pm V_{power\ supply}$ and is driven by the TTL signal. The output of the Op Amp signal drives a current injection system circuit.

METHODS AND MATERIALS

For a full list of parts, refer to Appendix A. The following were the principal electrical components

- LM741 Op Amp
- KMD15-1515 Power Supply
- 125 MΩ Precision Resistor
- 1 kΩ, 500 Ω, 180 Ω Resistors
- 10 kΩ Pot Trim Resistor
- 220 VAC 0.2A Fuse
- ADG411 IC Switch
- BNC Connectors (4) (insulated)
- SPDT (2)
- NTE956

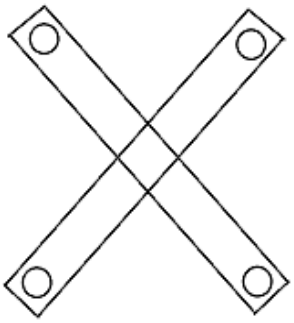
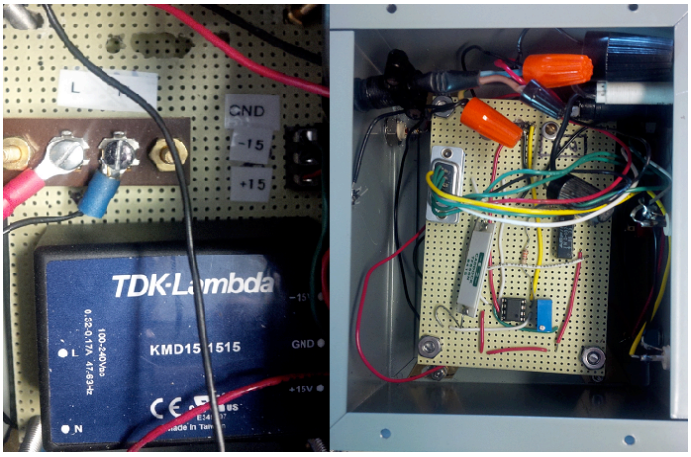


Figure 4: Mounting Design.

The casing of the voltage clamp instrument was metal with holes drilled into the front panel and the back panel for the installation of the BNC connectors, switches, a fuse and a power indicator LED. The components were then secured using nuts and the connections made to the rest of the circuit. The circuit was designed after researching voltage clamp designs. A relatively simple design was chosen for this project. Future improvements will be discussed in the Discussion section. Figure 3 shows the circuit that was chosen for the final design of the voltage clamp. We then constructed the circuit on a standard prototyping board without copper plating to limit failure due to oxidation of the components over time to extend the lifetime of the system. The biggest challenge was to find an efficient way to enclose the components inside while still allowing the circuit to be easily disassembled for future improvements or repair purposes. This was accomplished by using copper plates in an 'X' configuration (See Figure 4) so that the boards can be mounted with ease. The circuit was built in two portions, the first containing the Power supply and the second containing the Op Amp circuitry. The first prototyping board contained the power supply (Figure 5a) and a RS-232 connector was used to connect the ±15V supply to the board containing the Op Amp. The second prototyping board that was used included the main components for



(a) (b)

Figure 5: (a) First prototype board containing the power supply and (b) second prototype board containing the main circuit shown in Figure 3.

the Voltage Clamp (See Figure 5b). The components were soldered together and the inputs and output to the Op Amp were connected to the BNC using another RS-232 connector.

To prevent the AC signal from introducing unwanted noise in the system, the AC ground was connected to the chassis although this was not necessary for the Power Supply itself. The final unit after assembly is shown in Figure 6.

Figure 6: Final Unit Construction

RESULTS

The original and new voltage clamp instruments were compared by measuring current voltage relations in the same hypha of the *Neurospora crassa* with both instruments Two micropipettes filled with 3M KCl solution were impaled into the cell (Figure 7, *Left panel*) the resting potential of the cell was measured to be –110 mV. A computer program (Appendix C) provides the clamping voltage in bipolar ramp of specified duration. The program controlled the number of clamping steps and their duration, and activated the digital I/O TTL signal required to turn on the voltage clamp Op Amp. The clamped voltage and clamping current were observed on an oscilloscope and digitized for offline analysis. The data recorded by the computer was exported into an ASCII data file; the current-voltage relations were then analyzed by importing the data into Excel. Preliminary results showed that the new voltage clamp design had a wider output voltage range than the old design while there were no changes in the RMS noise or linearity. Figure 7 (*right panel*) shows the current voltage relations and current density –voltage relationships respectively of the old and new clamp designs.

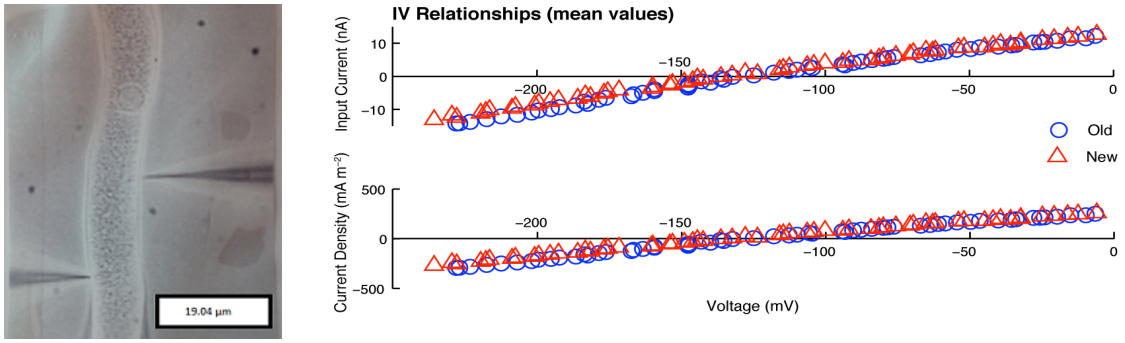
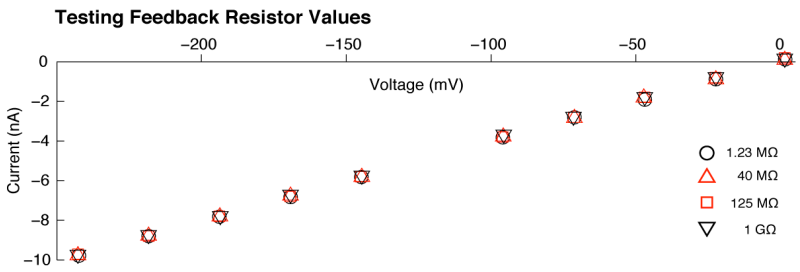


Figure 7: *Left Panel:* Cell Impalement using micropipettes. *Right Panel:* IV relations showing current voltage and current density-voltage relationships of the old (circles) and new (triangles) voltage clamp instruments.

Another critical aspect of this design was using a high enough negative feedback resistor value going from the output of the Op Amp back into the inverting input of the Op Amp to ensure a fast response time and high gain so that accurate readings of the current-voltage relationships can be made. The circuit was tested by installing the given feedback resistor values [1.23 MΩ, 40 MΩ, 125 MΩ, 1GΩ] in place of the 125 MΩ resistor being connected from pins 2 and 6 in Figure 1 and was then plotted on the same graph as shown in Figure 8. No difference was found between the different tested values.

Figure 8: Testing different feedback resistors to determine its effect on the current-voltage relationships of the voltage clamp design.



DISCUSSION

The data from Figure 7 was taken from the same hypha and measurements were taken consecutively to prevent variations in the data that may have been present from one hypha to another. Three measurements were taken for the old clamp and then the new voltage clamp was connected and another three measurements were made. Figure 7 shows the mean values of these three measurements. It was noted that in the new clamp design there appeared to be a slightly larger voltage range than the old design at negative voltages but no change on the upper end of the voltage range (0 mV). This variation was attributed to offsets inherent in the input bias current of the Op Amp circuit above and below 0 mA. Errors in the electrometer were not considered since they could not be quantitatively analyzed. Another interesting observation noted in Figure 7 was the clustering and non-uniform spread of the collected data points. Note that in both clamp designs, there appear to be 'gaps' in the data albeit some offset in the two designs. However, since the circuit constructed was only concerned with outputting a differential signal when the voltage at the inverting and non-inverting inputs varied, such discrepancies could not be attributed to the design here. Further investigation is necessary to find the root cause of this behavior.

A second consideration was the feedback resistor used to connect the output of the op amp to the inverting input of the op amp (125 MΩ resistor in Figure 1). Such a high value was used so that the circuit would respond instantaneously as the voltage was varied however; this is also limited by the slew rate of the Op Amp as well as the circuit used for the current injection. Note that resistor values even as low as 1.23 MΩ did not cause a corresponding change in the I-V relationship when tested against a model circuit of a cell. This is evident when considering equation 1 in conjunction with equations 2 and 3. A higher resistor value will not change the operation of the device; the circuit will still output a voltage clamped at $\pm V_{sat}$. One observation that was noted was that there was a slight but significant offset in the voltage as the resistor values were increased.

Table 1: Negative Feedback Resistor Values and the corresponding Input Current Offset.

Resistor Value	Input Current Offset (nA)
(1.23 ± 0.01) MΩ	0
(40 ± 0.004) MΩ	(0.0142 ± 0.005)
(125 ± 0.025) MΩ	(0.0568 ± 0.005)
(1 ± 0.04) GΩ	(0.1007 ± 0.005)

The variations in the input current offset are small and do not affect the I-V relationships for our measurements. Note that the current offsets were extracted from the equation of a line in the form of $y = mx + b$ using Matlab software. The values were then standardized in Table 1 with respect to the lowest resistor value (1.23 MΩ). The small difference in current offset were due to the offset potentiometer shown in Figure 3 not being adjusted for changes in negative feedback resistor values. Thus, these differences are expected for increasing values of resistors used and therefore using the values within the range given in Table 1 does not affect the functionality of the circuit in any way.

Table 2: RMS Error in the two designs.

	RMS	% Difference
Old Design	(18.8 ± 1) mV	6.6%
New Design	(17.6 ± 1) mV	

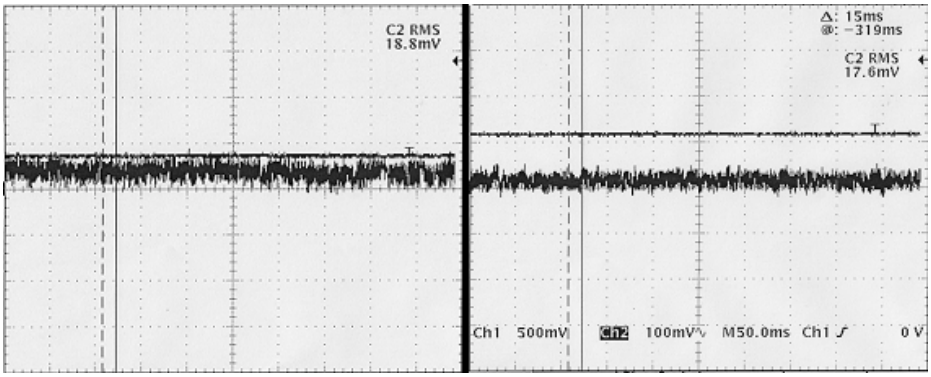


Figure 9: The RMS signal of the Old voltage clamp design (left) and New voltage clamp design (right).

Table 2 in conjunction with Figure 9 show the differences in RMS present in the two designs with a statistical difference of about 6.6%. These results may give a false representation of the noise control implemented in the system as the RMS values were found to fluctuate and even drift as a function of time and external noise sources such as nearby electromagnetic emitting devices (ex. computer monitor). The data collection of the I-V relationships is a much better indicator of the linearity as well as external noise sources than Table 2 and Figure 9.

Since the circuit operates essentially as a comparator, given a gain of 10^5, then the smallest difference between the inverting and non-inverting inputs to cause the output to go to saturation is given below.

$$A_v = gain = \frac{V_{sat}}{(V_+ - V_-)} \qquad (6)$$

$$(V_+ - V_-) = (15V / 10^5) = 150\mu V \qquad (7)$$

Due to the very small difference needed to drive this Op Amp configuration to saturation a comparator Op Amp theoretically can be used to achieve faster slew rates if all other parameters were constant. However, it is difficult to find comparators with very high impedances as is the case with standard differential Operational Amplifiers. Such designs may be considered in future revisions of the Voltage Clamp. The current injection circuit was not analyzed in this design and possible modifications of this system may lead to more dynamic I-V relationships with less ringing activity as was observed in this design.

REFERENCES

Analog Devices, “Precision Quad SPST Switchs”, ADG411/ADG412/ADG413 datasheet, 1998.

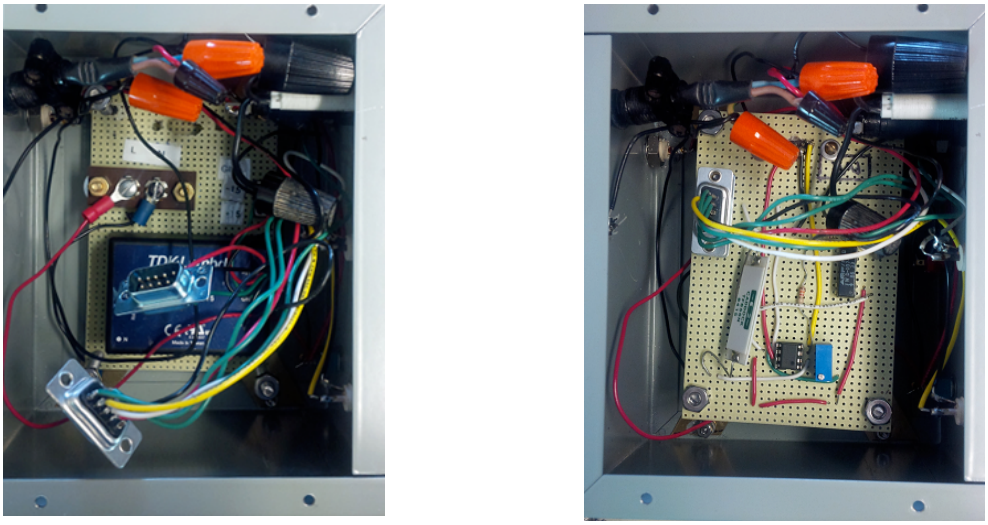
CADDOCK Electronics, Inc. “Type LF Low TC Ultra-Precision Film Resistors,” 125 Megaohms Film Resistor Datasheet, 2004.

National Semiconductor, “LM411 Low Offset, Low Drift JFET Input Operational Amplifier,” LM411 datasheet, April 1998.3

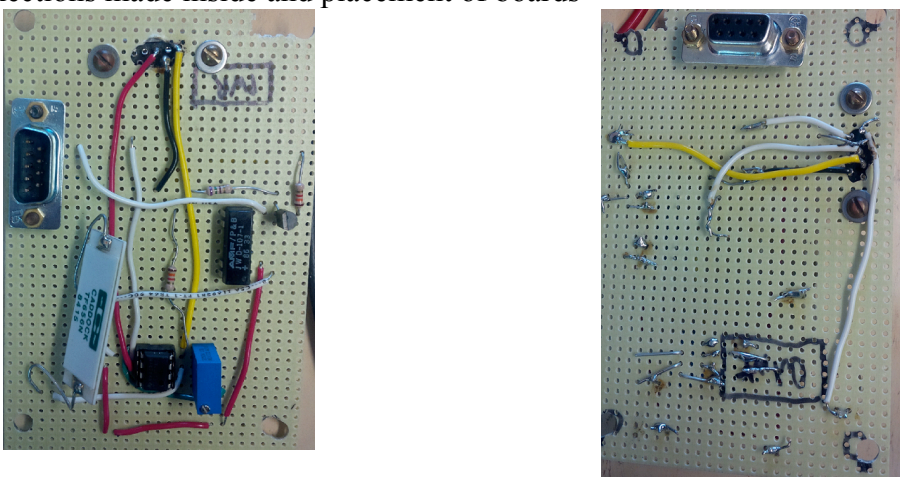
APPENDIX A – PARTS LIST

Part	Catalogue #	QTY	Cost
Power Supply +- 15V 500 mA	KMD15-1515	1	$60.50
Hammond Case (6 by 4 by 5 inches)	HM307-ND	2	$24.36
Toggle Switch – 125V input AC	450-1297-ND	4	$8.47 each
Toggle Switch -20VDC Rating	450-1522-ND	3	$4.58
Op-Amp (Lower Bandwidth, higher slew rate)	296-10415-5-ND	4	$2.55
Op-Amp (JFET Input Op Amp)	LF411CN	4	$1.44
Soldering Iron	WES51-120V-ND	1	$144.98
1/16 inch soldering tip -chisel	ETA-ND	1	$4.79
0.093 inch soldering tip - chisel	ETB-ND	1	$4.79
0.031 inch long conical soldering tip	ETO-ND	1	$4.79
Fuse Holder 5x20 mm	F1903-ND	2	$3.80
Fuse [250V 2A] Slow Blow Type	F3085-ND	2	$1.04
Wire – Black 22 AWG solid core 100 feet	C2004B-100-ND	1	$18.15
Wire- White 22 AWG solid core 100 feet	C2004W-100-ND	1	$18.15
Wire – Green 22 AWG solid core 100 feet	C2004G-100-ND	1	$18.15
Wire – Red 22 AWG solid core 100 feet	C2004R-100-ND	1	$18.15
22 AWG Red stranded wire – 7/30 conductor strand	C2016R-100-ND	1	$20.07
22 AWG Yellow stranded wire – 7/30 conductor strand	C2016Y-100-ND	1	$20.07
BNC Connectors	ARFX1064-ND	12	$2.02 each
Breadboard w/70 piece wire	438-1047-ND	2	$23.7 each
Circuit Prototype Board [4.5 by 3 inches]	3408K-ND	5	$8.90 each
Female D-Type 9 Pin Socket	A32510-ND	2	$4.10 each
Male D-Type 9 Pin Socket	A102056-ND	2	$2.68 each
15 V Reed Relay -7.5 mA coil current	DIP15-2A72-21	4	$.45
Transistors	P2N2222AGOS-ND	6	$0.43 each
DIP 8 Pin	A32361-ND	3	$0.60
Trimmer 10k +-10% tolerance 0.5W	3362P-103LF-ND	2	$1.19
Trimmer 20k +-10% tolerance 0.5W	3362P-203LF-ND	2	$1.19
Trimmer 10k +-5% tolerance 1.0 W	3250W-103-ND	2	$11.03
Trimmer 20k +-5% tolerance 1.0W	3250W-203-ND	2	$11.03
Light Indicator -110-125VAC	095-1363-09-311-ND	2	$15.24

APPENDIX B – MISC IMAGES



A1: Connections made inside and placement of boards

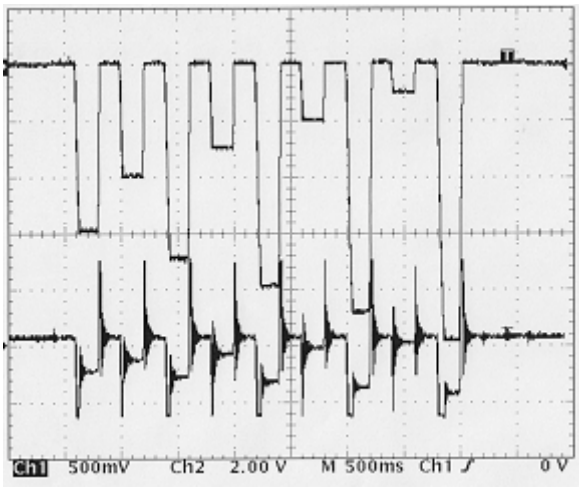


a *b*

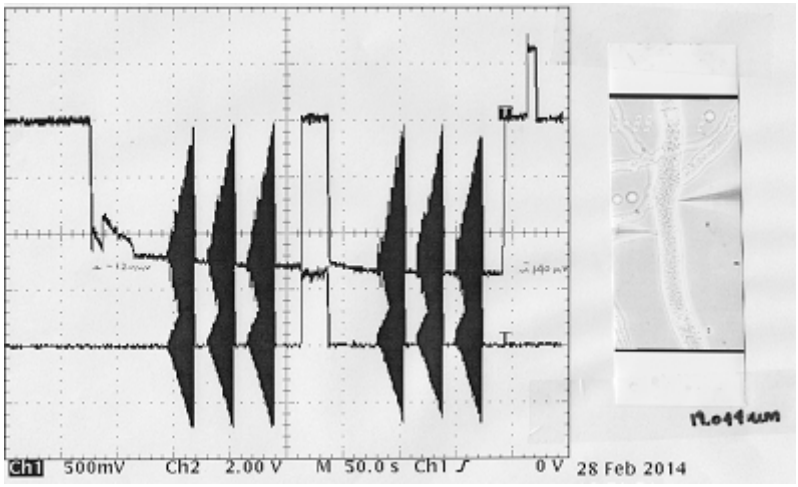
A2: Close up view of the (a) front and (b) back of the circuit shown in Figure 1.

a *b*

A3: Assembled units showing (a) the front panel and (b) the back panel with the power cable as well as a TTL BNC connector.



A4: The Voltage (top) and Current (bottom) data collection taken from the Oscilloscope for a model circuit of a cell.



A5: The Voltage (top) and Current (bottom) data collection taken from the Oscilloscope of *Neurospora crassa* hyphae. The image on the right taken from a Microscope at 40x shows the fungal tip impaled with two micropipettes.

APPENDIX C – C PROGRAM FOR VOLTAGE CLAMPING

```
#include <stdio.h>                  /*file read/write             */
#include <dos.h>                    /*file read/write             */
#DEFINE MASTER                      /*labpac declarations         */
#include "labhead.h"                /*I-V routine                 */
#include <time.h>

        main()
{
        FILE *input;                    /*file pointers               */
        int step, min, max, duration;   /*IV parameters               */

/*****************************************************************/
/*       input file for current-voltage measurement parameters    */
/*****************************************************************/

input = fopen("iv.prm","r");         /*opens file for read only   */
if (input == NULL){
        printf("Could not open %s\n", "iv.prm");
        exit(0);
        }
while (!feof(input)) {
        fscanf(input, "%d %d %d %d", &step, &min, &max, &duration);
        IV(step, min, max, duration);
        exit(0);
        }
}

/*****************************************************************/
/* I-V data measurement                                          */
/*****************************************************************/

IV(step, min, max, duration)
{
        int V_clamp[100];
        int V_rest;
        float V[100], I[100];           /*IV datafile variables       */
        int n, increment, midpoint;     /*V_clamp calculations        */
        int i, Vin, Iin;                /*V and I input averaging     */
        char *file_out;
        FILE *output;
        struct date datebuf;
        struct time timebuf;
        int channel=0;


/*****************************************************************/
/* Labpac initialization - LABPAC.COM must be invoked !!!         */
/*****************************************************************/

labpac(RESET);
labpac(TIINIT, TIMER);
labpac(AIINIT, ATOD, 2, 1, 1);
labpac(AOINIT, DTOA, 2);
labpac(DINIT, PIO, 3);
V_rest = labpac(AIRAW, 0);                  /*reads Vrest from Ch*/

/*****************************************************************/
/* Calculation of V_clamp                                        */
/*****************************************************************/

increment = (max - min) / step;
midpoint = (max + min) / 2;

for(n = 1; n <= (step * 2) + 1; n++) {
        if(n%2 != 0) V_clamp[n] = V_rest;           /* odd n clamps V_*/
        else if((n/2)%2 != 0)                       /*odd n/2 clamps  */
        V_clamp[n] = (midpoint - (n/4.0+0.5) * increment);
        else                                        /*even n/2 clamps */
        V_clamp[n] = (midpoint + (n/4) * increment);
        }
```

```
/*****************************************************************/
/* Now we can run the I-V measurement                            */
/*****************************************************************/
for (n = 1; n <= step * 2 + 1; n++) {
                                        /*timer 5, counting a */
       labpac(TIST, 5, 14, 0);                /*1 kHz (1 msec) with */
       labpac(DOSET, channel, 16);            /*each duration (msec */
       labpac(AORAW, 0, V_clamp[n]);          /*V_clamp on Ch 0     */
              if(n%2 == 0) {
              labpac(TIST, 4, 14, 0);
              labpac(TISTAT, 4, duration - 10);
          for(i=1, Vin=0, Iin=0; i<=5; i++){
               Vin += labpac(AIRAW, 0);   /*Clamped voltage     */
               Iin += labpac(AIRAW, 1);   /*Clamping current    */
               }
               V[n] = Vin/5;
               I[n] = Iin/5;
              }
       labpac(TISTAT, 5, duration);
}
labpac(AORAW, 0, V_rest);
labpac(DOCLR, channel, 16);
labpac(AORAW, 0, 0);

/*****************************************************************/
/* I-V data written to datafile on drive A                       */
/*****************************************************************/

getdate(&datebuf);
gettime(&timebuf);
file_out = tempnam("c:","IV");
output = fopen(file_out, "w");        /*opens file for write only*/
              if (output == NULL){
              printf("Could not open datafile %s\n", file_out);
              exit(0);
              }
              for (n = 1; n <= step * 2 + 1; n++) {
              if(n%2 == 0 )
              fprintf(output, "%.2f %.2f \n", V[n] / 2.0475, I[n] / 2.0475);
              }
fprintf(output, "~ \n");
fprintf(output,"%.2d/%.2d/%.2d  %.2d:%.2d:%.2d  %s\n",
              datebuf.da_mon,datebuf.da_day,datebuf.da_year,
              timebuf.ti_hour,timebuf.ti_min,timebuf.ti_sec,file_out);
fprintf(output, "Resting Potential: %.2f\n", V_rest/2.0475);
}
```